IFW

Attorney Docket: 33851/41886
PATENT

NOV 28 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor	Dustin A. Woodbury	Confirmation No.	6517
Serial No.	10/798,559	Art Unit:	2818
Filing Date	March 12, 2004	Examiner	LE, Thao P.

Title: **METHOD AND STRUCTURE FOR NON-SINGLE-POLYCRYSTALLINE CAPACITOR IN AN INTEGRATED CIRCUIT**

AMENDMENT

Barnes & Thornburg Customer No:
23646
U.S. Patent and Trademark Office

Mail Stop Amendments
U.S. Patent and Trademark Office
Box 1450
Alexandria, VA 22314-1450

In response to the official Patent Office action dated August 30, 2005, please amend the claims as shown in the attached Claims Summary.

Claims 1-12 stand rejected under 35 U.S.C. 102(b) as being anticipated by Chi, U.S. Patent 5,173,437. This rejection is respectfully traversed.

Claim 1 is directed to a method of forming a capacitor in an integrated circuit including forming a first non-single-crystalline layer on a gate dielectric layer on a surface of the integrated. A capacitor dielectric layer is formed on the first non-single-crystalline layer and a second non-single-crystalline layer is formed on the capacitor dielectric layer. Portions of the second non-single-crystalline layer is removed to define a top plate of the capacitor; portions of the capacitor dielectric layer are removed to define a dielectric of the capacitor; and portions of the first non-single-crystalline layer are removed to define a bottom plate of the capacitor after a top plate is defined on the gate dielectric.

The process Chi forms the first poly layer 56 on field oxide 54 and the gate oxide 54. The ultimately formed capacitor is formed over the field oxide 52 and not on the gate oxide 54. The gate oxide is only used in the field effect transistor illustrated in Figures 7 and 8. Thus Chi cannot anticipate nor is it obvious to modify Chi to produce the claims of the present invention. As noted, Claim 1 specifically requires forming the gate dielectric layer on the surface of the substrate of an integrated circuit and forming the first non-single-crystalline layer on the gate dielectric layer. Portions of the first non-single-crystalline layer are